REMARKS

These remarks are in response to the fourth, final Office Action mailed on September 11, 2002. The Office Action rejected claims 3-11, 15-25, 36-39 and 43-64 under 35 U.S.C. 112, second paragraph, and all of the pending claims under 35 U.S.C. 103(a) under several different combinations of references as discussed below. Claims 3, 4, 15, 26, and 36 have been amended, claims 40-71 have been cancelled, and several new claims have been added.

Rejections under 35 U.S.C. 112, second paragraph

Of the non-cancelled claims, claims 3, 4, 15, and 36 along with their dependent claims were rejected under 35 U.S.C. 112, second paragraph. Although it is believed that the claims were acceptable and their meaning clear in their original form, the "resultant structure" language has been replaced in all of these claims with a description of this structure, thereby removing the basis of these rejections.

Rejection of claims 3-11 and 36-39 under 35 U.S.C. 103(a)

Claims 3, 8-11, 36, and 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (US 5,683,931) in view of Bencher, with claims 4-7 also rejected in view of Wang et al. (US 5,545,585). (Specific reasons for the further rejection of claims 37 and 38 are not explicitly stated in the Office Action.) Although these claims are believed allowable for the various reasons previously stated, independent claims 3, 4 and 36 have been amended in the present response in order to further distinguish them from the prior art.

As discussed in the present application, a major aspect of the present invention is the ability to lessen the effects caused by the undercutting of the capacitor dielectric, as indicated at 180 in Figure 3 and discussed on page 10, lines 26-30, and page 4, line 25, to page 6, line12, of the present application. This results during the etch of dielectric layer 160, when, in addition to the portion whose removal is desired, a portion of the dielectric layer between the upper electrode 140 and the conducting layer 120 (from which the lower

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

electrode will be formed) is removed. In the embodiment of claims 3-11 and 36-39, a conformal dielectric layer (170, Figure 4) is formed and enters into this inter-plate region, thereby avoiding the various problems that result if the anti-reflective layer (190, Figure 4) is allowed into the inter-plate region.

Neither the occurrence of this inter-plate undercutting (180, Figure 3) nor the subsequent introduction of a conformal dielectric layer into this inter-plate region is found in the prior art. Further, it not believed to be obvious or suggested from the prior. (For example, in the Becher reference the stress is upon the use of a *dielectric* antireflective coating, where here the problem is that the anti-reflective layer is not dielectric enough, but rather is too conductive.) This is reflected in independent claims 3, 4, and 36. For example, claim 3 contains the language:

> ...subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;
>
> subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region...,

where the underlined portions have been added. Claims 4 and 36 contain similar language and have been similarly amended. Consequently, claims 3, 4, and 36, along with dependent claims 5-11 and 37-39 are believed allowable.

Rejection of claims 15-25 under 35 U.S.C. 103(a)

Claims 15, 16, and 19-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma et al. (US 5,397,729) in view of Bencher, with claims 16 and 17 further rejected in view of Patel et al. (US 5,374,578) and Wang, respectively. Claims 15-25 are described in the application with respect to Figures 6-9. As shown in these figures, in the process of forming the side-wall spacers (185, Figure 8), an oxide layer 175 is formed over the upper electrode 140 in Figure 7, and then etched back, resulting in the side-wall spacers 185 and *exposing the top of the upper electrode* 140, as shown in Figure 8.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

This process is distinct from the process as shown in Figures 4A-F of Kayanuma, as cited in the Office Action. As shown there in Figure 4C, an oxide layer 57 is formed over the upper electrode 54 and *maintained there* in the subsequent steps, particularly the etch performed between Figures 4C and 4D using the resist 58. The maintaining of this oxide layer 57 over the top electrode 54 is an important aspect of the teachings of Kayanuma, as it is needed in the etch performed between Figure 4E and 4F, where the resist 60 is used to defined the transistor gate (59, 52) but the layer 57 protects the capacitor structure when the layer 59 is etched away. This is described at column 9, lines 23-34. Consequently, Kayanuma teaches away from removal of the dielectric layer (175 in the application, 57 in Kayanuma) from over the top electrode, as is done in the present application.

This difference is reflected in the claims. Claim 15 states:

> ...removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;
>
> forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;
>
> removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode layer and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric and wherein the top of the top electrode is exposed...,

where the underlined portion has been added by the current Amendment. Consequently, claim 15 and its dependent claims, claims 16-25 are respectively submitted to be allowable.

Rejection of claims 26-30 under 35 U.S.C. 103(a)

The Office Action rejected claims 26-30 under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US 5,618,749) in view of Bencher. As shown in Figure 7 of Takahashi `749, a poly layer 6a is formed over the dielectric layer 1, which is in turn formed over poly layer 2. The poly layer 6a *and* dielectric layer 1 are *both* then etched back to the lower electrode layer 2, except for the capacitor structure, as shown in Figure 8.

This is distinct from the third embodiment of the present invention, as described on page 11, lines 11-30, of the present application. According to the present invention, this embodiment of the present invention defines and etches the top electrode layer, but leaves the dielectric layer in place over the lower electrode layer prior to forming the

LAW OFFICES OF
SKJERVEN MORRILL LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

dielectric layer. This difference is again reflected in the claims. Claim 26 contains the limitation:

> ...removing a portion of said top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed...

where the underlined portion has again been added in this Amendment. Consequently, claims 26-30 are also respectfully submitted to be allowable over the prior art.

New claims

The present Amendment also adds several new claims. New claims 72-80 are all dependent claims are add detail concerning the anti-reflective layer.

An important aspect of the first embodiment of the present invention is the inclusion of a capacitor module (steps 4-10a of page 9) within process flow without the need to reformulate the process parameters of the non-capacitor stages. As described from page 8, line 16, to page 12, line 18, this allows the parameters associated with the photolithographic process (including the anti-reflective layer) to be optimized for the case when the capacitor module is absent. The capacitor module is then itself optimized while maintaining its modular aspect, so that it can be included or omitted according to the process needs. New claims 81-85 are drawn to this aspect of the present invention.

Conclusion

For any of these reasons, reconsideration of the Office Action's rejection of claims 3-11, 15-30, and 36-39, and consideration of new claims 72-85, is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

EXPRESS MAIL LABEL NO:

EV259159804US

Respectfully submitted,

Michael G. Cleveland
Reg. No. 46,030

12-11-02
Date

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

APPENDIX

Amended Claims

3.(Thrice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the [resultant structure subsequent to forming said] conformal insulating layer.

4.(Thrice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of [resultant structure subsequent to forming said] conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

15.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode layer and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric and wherein the top of the top electrode is exposed; and

forming a non-insulating layer over at least a portion of the [structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer]

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

top electrode, the side wall spacers and the lower electrode layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.

26.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

36.(Twice Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, whereby a portion of said conformal layer is formed in the region between the top electrode and the conductive layer;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the [structure resultant from said forming a] conformal layer;

forming a patterned mask over the [structure resultant from said forming an] ARL; and

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

etching said conductive layer using said patterned mask.

Pending Claims

(Claims 1 and 2 have been cancelled.)

3.(Thrice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conformal insulating layer.

4.(Thrice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

5. The method according to claim 4, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

6. The method according to claim 5, wherein said thermal process is a rapid thermal oxidation is performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range of from 850°C to 1050°C.

7. The method according to claim 4, wherein said conformal insulating layer is formed by deposition.

8. The method of claim 3, wherein said ARL is an anti-reflective coating.

9. The method of claim 3, wherein said ARL is titanium nitride.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

10. The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. The method according to claim 10, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

(Claims 12-14 have been cancelled)

15.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode layer and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric and wherein the top of the top electrode is exposed; and

forming a non-insulating layer over at least a portion of the [structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer] top electrode, the side wall spacers and the lower electrode layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.

16. The method according to claim 15, wherein said insulating layer is formed by deposition.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

17.(Amended) The method according to claim 16, wherein prior to forming said insulating layer by deposition, an anneal is performed.

18. The method according to claim 15, wherein said insulating layer is grown.

19. The method according to claim 15, wherein said insulating layer is an oxide layer with a thickness in the range of from 500Å to 2000Å.

20. The method according to claim 15, wherein said side wall spacers have a width in the range of from 500Å to 2000Å.

21. The method according to claim 15, wherein said ARL is an anti-reflective coating.

22. The method according to claim 15, wherein said ARL is titanium nitride.

23. The method according to claim 15, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

24. The method according to claim 23, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

25. The method according to claim 15, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

26.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

27. The method according to claim 26, wherein said ARL is an anti-reflective coating.

28. The method according to claim 26, wherein said ARL is titanium nitride.

29. The method according to claim 26, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

30. The method according to claim 26, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

(Claims 31-35 have been cancelled.)

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

36.(Twice Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, whereby a portion of said conformal layer is formed in the region between the top electrode and the conductive layer;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the [structure resultant from said forming a] conformal layer;

forming a patterned mask over the ARL; and

etching said conductive layer using said patterned mask.

37. The method according to claim 36, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

38. The method according to claim 37, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

39. The method according to claim 36, wherein said conductive layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

(Claims 40-71 have been cancelled)

72.(New) The method of claim 3, further comprising:

forming a photoresist over at least a portion of the anti-reflective layer; and

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

73.(New) The method of claim 72, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

74.(New) The method of claim 3, wherein said anti-reflective layer is a Si_xON_y film.

75.(New) The method of claim 15, further comprising:

forming a photoresist over at least a portion of the anti-reflective layer; and

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more.

76.(New) The method of claim 75, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

77.(New) The method of claim 15, wherein said anti-reflective layer is a Si_xON_y film.

78.(New) The method of claim 26, further comprising:

forming a photoresist over at least a portion of said anti-reflective layer;

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more; and

subsequently etching a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer using said photoresist, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

79.(New) The method according to claim 78, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

80.(New) The method according to claim 26, wherein said anti-reflective layer is a Si_xON_y film.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

81.(New) A method of forming an integrated circuit, comprising:

a process flow for forming one or more transistors including:

forming a conductive layer on a semiconductor body;

subsequently forming an anti-reflective layer; and

defining and etching the conductive layer using the anti-reflective layer; and

an optional capacitor process module including, subsequent to said forming a conductive layer and prior to said forming an anti-reflective layer:

forming a top capacitor electrode over a portion of said conductive layer; and

forming a dielectric layer between said top electrode and said conductive layer, wherein said defining and etching the conductive layer forms the gate of one or more transistors and a bottom capacitor electrode,

wherein the process parameters of said process flow for forming one or more transistors are optimized for the case when the optional capacitor process module is omitted, and wherein the process parameters for the optional capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized for the case when the capacitor process module is omitted.

82.(New) The method of claim 81, wherein said optional capacitor process module comprises:

forming a dielectric layer over at least a portion said conductive layer;

forming a top electrode layer over at least a portion of said conductive layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming said top capacitor electrode;

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said conductive layer, thereby forming said dielectric layer between said top electrode and said conductive layer; and

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the conductive layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer.

83.(New) The method of claim 82, wherein the thickness of said conformal insulating layer is selected to optimize the capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized for the case when the capacitor process module is omitted.

84.(New) The method of claim 82, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

85.(New) The method of claim 81, wherein said defining and etching the conductive layer using the anti-reflective layer comprises:

forming the anti-reflective layer over the conductive layer and, when the optional capacitor process module is included, the top capacitor electrode and the dielectric layer between said top electrode and said conductive layer;

forming a patterned mask over the anti-reflective layer; and

and etching said conductive layer using said patterned mask.

LAW OFFICES OF
SKJERVEN MORRILL LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646